(12) UK Patent Application (19) GB (11) 2 321 804 (13) A

(43) Date of A Publication 05.08.1998

(21) Application No 9725431.2

(22) Date of Filing 01.12.1997

(30) Priority Data
(31) 970055 (32) 29.01.1997 (33) IE

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(51) INT CL$^6$
H02M 3/07

(52) UK CL (Edition P )
H2F FCP

(56) Documents Cited
GB 2244392 A US 5627739 A

(58) Field of Search
UK CL (Edition P ) H2F FCP FXS FXT FXX
INT CL$^6$ G05F 3/20 , G11C 5/14 16/06 , H02M 3/07
Online: WPI

(54) Abstract Title
**A charge pump circuit**

(57) A charge pump circuit comprises a load capacitor ($C_l$) across which an output voltage of approximately twice the supply voltage ($V_s$) is provided. A pump capacitor ($C_p$) is charged from the supply voltage ($V_s$) through first and second charge switches (SC1,SC2), and a first pump switch (SP1) raises the voltage on the pump capacitor ($C_p$) to twice the supply voltage ($V_s$), which is then in turn applied to the load capacitor ($C_l$) through a second pump switch (SP2). The switches (SC1,SC2,SP1,SP2) are each provided with a high resistance switch (SR1) and a low resistance switch (SR2) parallel to each other. A select pin ($P_1$) of the switches (SC1,SC2,SP1,SP2) alternatively selects the high resistance (SR1) and the low resistance switch (SR2). On initial charging of the capacitors ($C_l$,$C_p$) the high resistance switches (SR1) are selected for minimising the initial current drawn from the supply voltage ($V_s$), and after the capacitors ($C_l$,$C_p$) have been initially charged, the high resistance switches (SR1) are deselected and the low resistance switches (SR2) are selected for steady state operation of the charge pump circuit. An additional charge pump stage may be added (Fig 2).

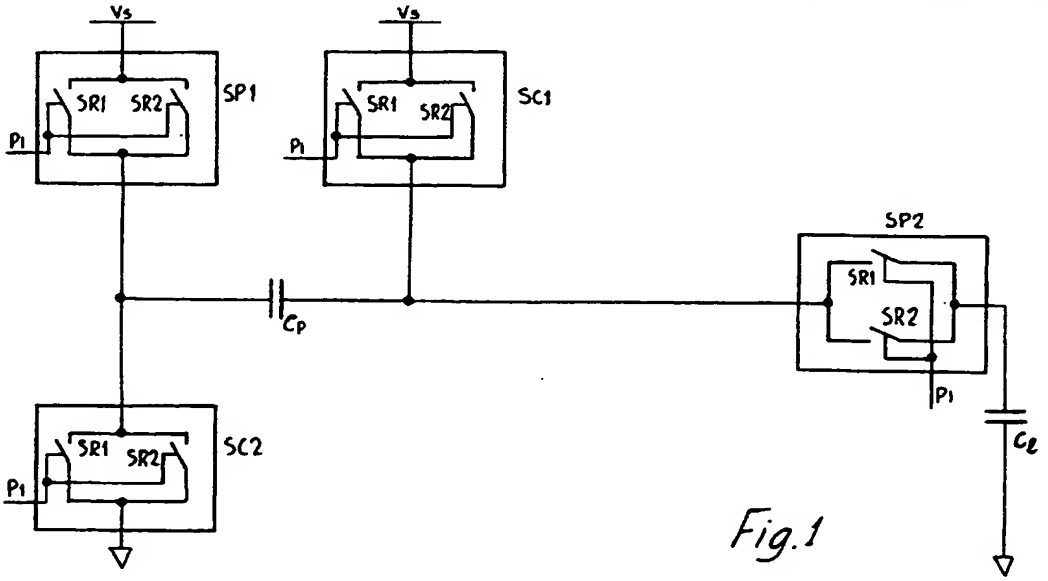


Fig.1

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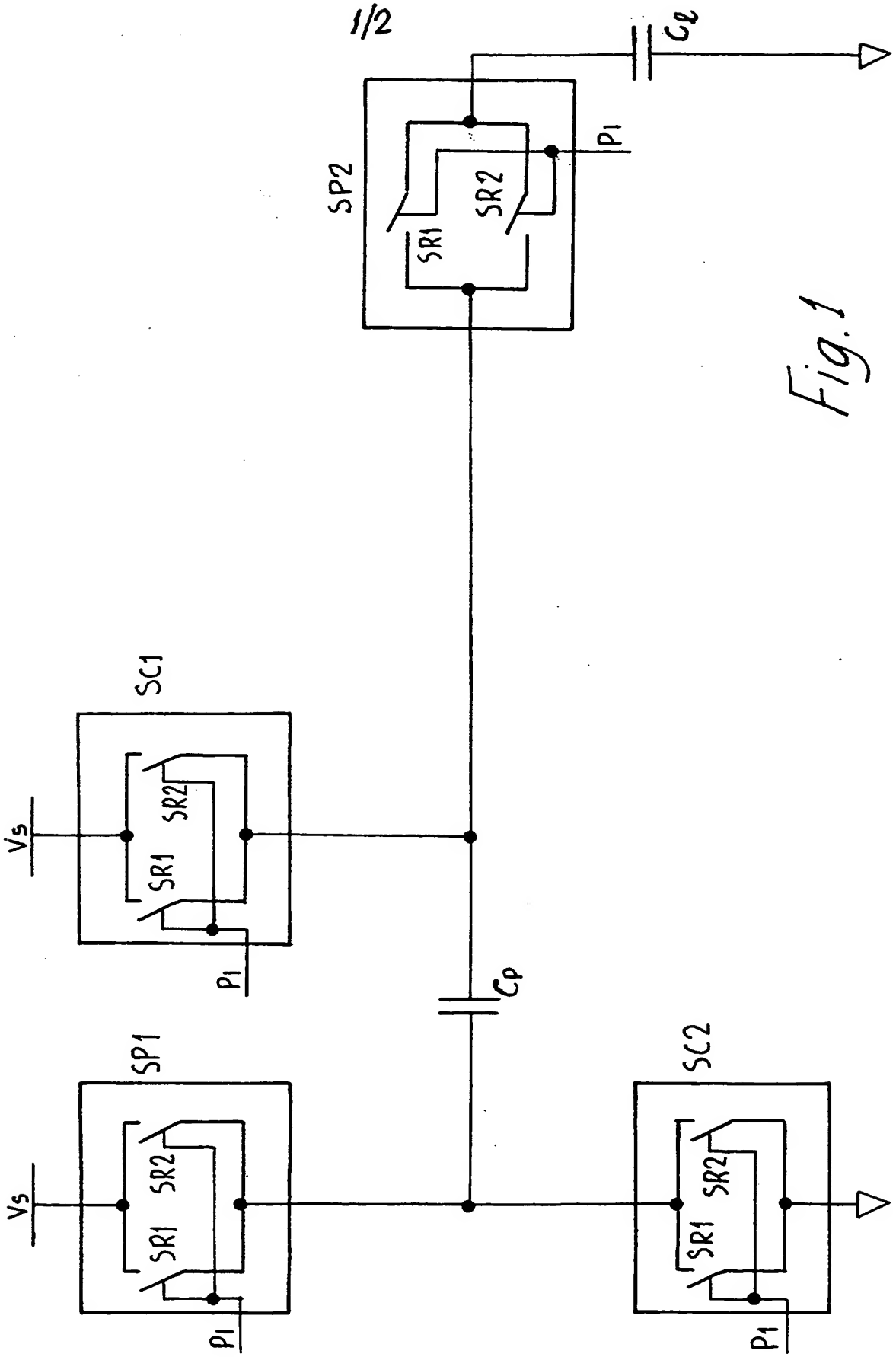


Fig. 1

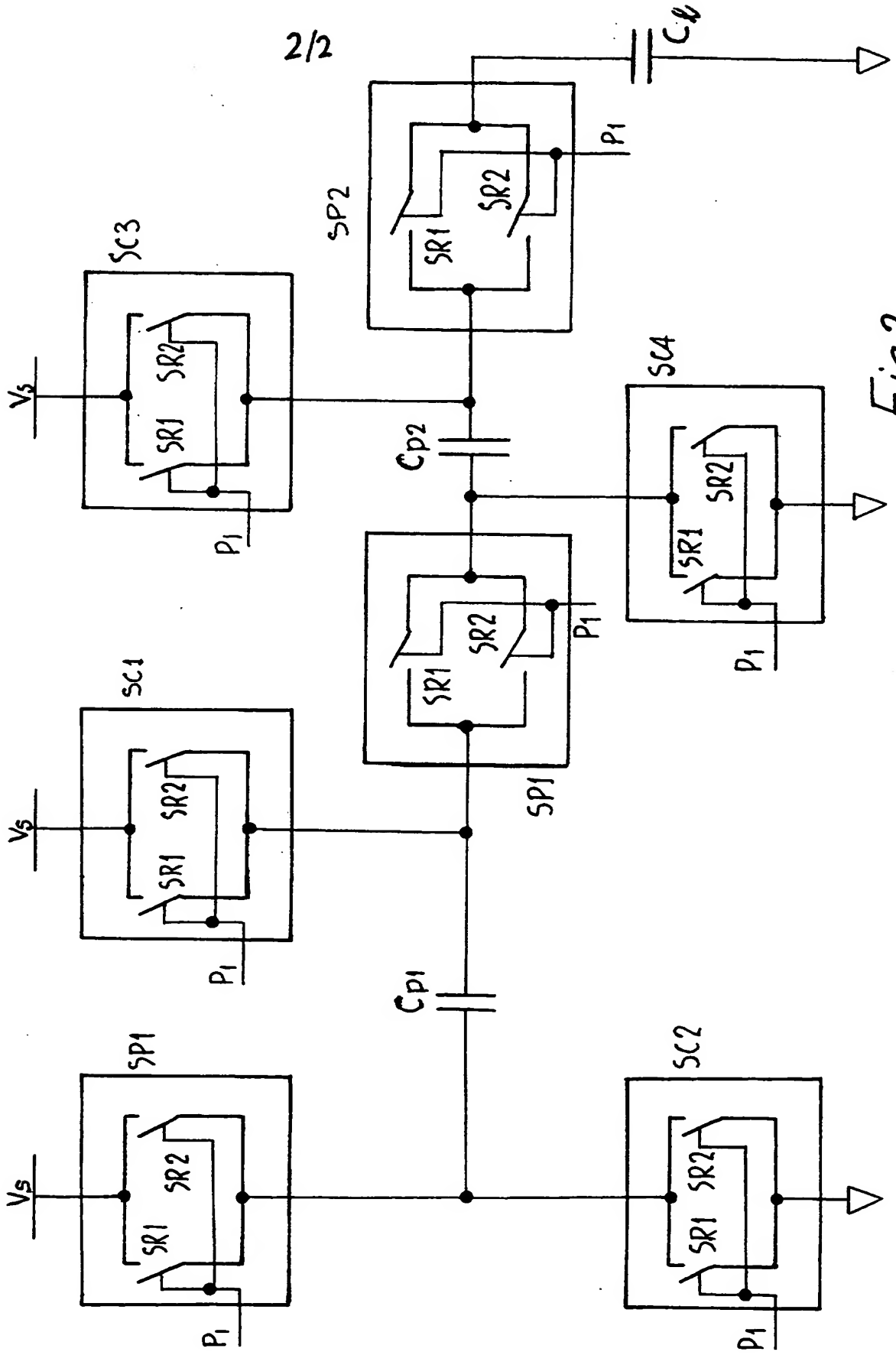


Fig.2

"A charge pump circuit"

The present invention relates to a charge pump circuit, and in particular, though not limited to a charge pump circuit for use in solid state circuitry, and the invention also relates to a circuit comprising the charge pump circuit.

Charge pump circuits provide a high voltage output load supply from a low voltage primary source. They are typically used where precise output voltage control is not required and the output voltage may vary within reasonable limits. Charge pump circuits comprise a load capacitor, across which the high output load voltage is provided, and one or more charge capacitors, which are simultaneously charged from the voltage source, and on being charged, the charge is then applied to the load capacitor for raising the voltage across the load capacitor to the desired high output voltage, or for maintaining the voltage of the load capacitor at the desired high output voltage.

In general, charge pump circuits generate relatively large switch currents, in particular, during power-up when both the pump capacitor or capacitors and the load capacitor are being charged from zero voltage to their steady state values. The large switch currents are

limited only by the series switch resistances of the respective switches which must be maintained at relatively low resistance values in order to prevent unacceptable losses during normal steady state operation.

The large switch currents cause a number of problems, in particular, they induce voltage ripple on the supply voltage from the voltage source, and cause excessive electromagnetic and radio frequency interference which induce noise in other circuits associated with the charge pump circuit. The problem with voltage ripple on the supply voltage is particularly serious where the primary voltage supply is derived from a battery. In general, low power batteries contain significant internal resistance, and a high switch current can cause the battery voltage, and in turn, the supply voltage to drop significantly, and in many instances to drop to a level below the operating level of other circuits associated with the charge pump circuit, thereby causing erroneous operation of the circuitry. In instances where under voltage detection and an under voltage lock out circuit is provided, the circuitry can inadvertently shut down.

One known method for minimising voltage ripple on the primary supply voltage and for minimising noise induced

by electromagnetic and radio frequency interference is to add a decoupling capacitor to the primary supply voltage. However, this significantly increases the cost of providing a charge pump circuit, which itself is, in general, a relatively low cost circuit.

There is therefore a need for a charge pump circuit in which voltage ripple on the primary supply voltage induced by the charge pump circuit is minimised, and also preferably, electromagnetic and radio frequency interference is likewise minimised.

The present invention is directed towards providing such a charge pump circuit, and a circuit comprising the charge pump circuit.

According to the invention there is provided a charge pump circuit comprising at least one pump capacitor, and a load capacitor, a charge path for charging the pump capacitor, and a pump path for charging the load capacitor to an output voltage which is above the supply voltage, wherein each of the charge paths and the pump paths comprises a high resistance path and a low resistance path in parallel with each other, the high resistance and low resistance paths of the respective charge and pump paths being selectively operable so that initial charging of the pump capacitor

and initial charging of the load capacitor to the output voltage is through the high resistance paths of the respective pump and charge paths, and charging of the pump capacitor and the load capacitor during steady state operation of the circuit is through the low resistance paths of the respective pump and charge paths.

In one embodiment of the invention each high resistance path comprises at least one high resistance element.

In another embodiment of the invention the charge path comprises a first charge switch means and a second charge switch means in series with the pump capacitor for respectively connecting the pump capacitor to the supply voltage and to ground for charging the pump capacitor.

Preferably, at least one of the first and second charge switch means comprises a high resistance switch means and a low resistance switch means in parallel with each other for forming the high resistance path and the low resistance path, respectively, of the charge path. Advantageously, both the first charge switch means and the second charge switch means each comprise a high resistance switch means and a low resistance switch means in parallel with the high resistance switch means

for forming the high resistance path and the low resistance path, respectively, of the charge path.

In another embodiment of the invention the pump path comprises a first pump switch means in series with the pump capacitor and the load capacitor for connecting the pump capacitor to the supply voltage for raising the voltage of the pump capacitor above the supply voltage, for in turn charging the load capacitor to the output voltage.

Preferably, the first pump switch means comprises a high resistance switch means and a low resistance switch means in parallel with each other for forming the high resistance path and the low resistance path, respectively, of the pump path.

In a further embodiment of the invention a second pump switch means is provided in series with the pump capacitor and the load capacitor for selectively connecting the respective capacitors together for charging the load capacitor. Advantageously, the second pump switch means comprises a high resistance switch means and a low resistance switch means in parallel with each other for forming the high resistance path and the low resistance path, respectively, of the pump path.

In one embodiment of the invention each high resistance switch means comprises a high resistance transistor switch, and each low resistance switch means comprises a low resistance transistor switch.

In another embodiment of the invention the respective high and low resistance transistor switches are solid state switches.

Preferably, each charge switch means and each pump switch means is responsive to a select signal for simultaneously selecting the high resistance switch means and deselecting the low resistance switch means.

In another embodiment of the invention a plurality of pump capacitors are connected in series with the load capacitor in the pump path, and each pump capacitor is provided with a charge path having a high resistance path and a parallel low resistance path.

Additionally, the invention provides a circuit comprising the charge pump circuit according to the invention, and a control means for issuing a select signal for selecting one of the high resistance and low resistance paths of the respective pump and charge paths.

Preferably, the control means is implemented in software in a microprocessor, the select signal being provided on an output pin of the microprocessor.

The invention will be more clearly understood from the following description of some preferred embodiments thereof which are given by way of example only with reference to the accompanying drawings, in which:

Fig. 1 is a circuit diagram of a charge pump circuit according to the invention, and

Fig. 2 is a circuit diagram of a charge pump circuit according to another embodiment of the invention.

Referring to the drawings and initially to Fig. 1, there is illustrated a charge pump circuit according to the invention indicated generally by the reference numeral 1 for providing a high output voltage $V_h$ across a load capacitor $C_1$ which is derived from a low voltage supply voltage $V_s$, which typically is in turn derived from a battery source. In this embodiment of the invention the supply voltage $V_s$ is approximately three volts, and the high output voltage $V_h$ across the load capacitor $C_1$ is approximately six volts. The load capacitor $C_1$ and a pump capacitor $C_p$ are initially

charged from the supply voltage $V_s$. The voltage on the pump capacitor is raised above the supply voltage to the output voltage, and its charge is subsequently applied to the load capacitor $C_l$ for raising the voltage of the load capacitor $C_l$. The pump capacitor $C_p$ is charged to the supply voltage through a charge path which comprises a first charge switch means, namely, a first charge switch SC1 and a second charge switch means, namely, a second charge switch SC2. The first charge switch SC1 connects a first plate of the pump capacitor $C_p$ to the supply voltage $V_s$, while a second charge switch SC2 connects a second plate of the pump capacitor $C_p$ to ground.

The pump capacitor $C_p$ and the load capacitor $C_l$ are connected in series in a pump path for raising the voltage of the pump capacitor $C_p$ to the output voltage, and for in turn charging the load capacitor $C_l$ to the output voltage $V_h$. The pump path comprises a first pump switch means, namely, a first pump switch SP1 and a second pump switch means, namely, a second pump switch SP2 in series with the pump capacitor $C_p$ and the load capacitor $C_l$. The first pump switch SP1 connects the second plate of the pump capacitor $C_p$ to the supply voltage $V_s$ when the pump capacitor $C_p$ has been charged to the supply voltage $V_s$ for raising the voltage on the first plate of the pump capacitor $C_p$ to the output

voltage approximately. The second pump switch SP2 connects the pump capacitor $C_p$ to the load capacitor $C_1$ for raising the voltage across the load capacitor $C_1$ to the output voltage, after the voltage on the pump capacitor $C_p$ has been raised to the output voltage. The second pump switch SP2 also connects the load capacitor $C_1$ to the supply voltage $V_s$ through the first charge switch SC1 for initial charging of the load capacitor $C_1$ to the supply voltage on power up of the charge pump circuit 1.

Each switch SC1, SC2, SP1 and SP2 is a solid state switch, and each comprises a high resistance switch means, namely, a high resistance switch SR1, and a low resistance switch means, namely, a low resistance switch SR2, which respectively form a parallel high resistance path and a low resistance path in each of the charge path and pump path. The high resistance switches SR1 and the low resistance switches SR2 are alternately operable by a select signal which is derived from a control means, which may be a dedicated control circuit, or other circuitry with which the charge pump circuit 1 is associated. In this embodiment of the invention each high and low resistance switch SR1 and SR2, respectively, is provided by a field effect transistor, the high and low resistance switches SR1 and SR2, respectively, of each

switch SC1, SC2, SP1 and SP2 being implemented by integrated circuits, and typically the select signal is derived from a microprocessor from an associated circuit. A select pin $P_1$ is provided on each switch SC1, SC2, SP1 and SP2 for receiving the select signal for selecting the high resistance switches SR1 of the switches SC1, SC2, SP1 and SP2.

Initial charging of the pump capacitor $C_p$ and initial charging of the load capacitor $C_1$ to the output voltage of six volts is carried out through the high resistance path of the charge path and the pump path, namely, through the high resistance switches SR1 of the first and second charge and pump switches SC1, SC2, SP1 and SP2, as will be described below for minimising the current drawn during initial charging of the pump capacitor $C_p$ and the load capacitor $C_1$. Once the pump and load capacitors $C_p$ and $C_1$ have been fully charged, and the voltage across the load capacitor $C_1$ has been raised to the output voltage of six volts approximately, the select signal is deactivated for simultaneously selecting the low resistance path of the charge path and pump path for steady state operation of the circuit. In other words, the select signal is deactivated on the pins $P_1$ of the switches SC1, SC2, SP1 and SP2 for simultaneously selecting the low resistance switches SR2 and deselecting the high resistance

switches SR1.

Operation of the charge pump circuit 1 will now be described. Prior to power up of the charge pump circuit 1 the load capacitor $C_l$ and the pump capacitor $C_p$ are at zero volts. On power up, the select signal is applied to the select pins $P_l$ of the first and second charge and pump switches SC1, SC2, SP1 and SP2, respectively, for selecting the high resistance switches SR1 and deselecting the low resistance switches SR2 of the switches SC1, SC2, SP1 and SP2. Initially, the first and second charge switches SC1 and SC2 are operated and the second pump switch SP2 is operated for connecting the pump capacitor $C_p$ to the supply voltage $V_s$ and ground, and the load capacitor $C_l$ to the supply voltage $V_s$ and ground, thus charging the load capacitor $C_l$ and the pump capacitor $C_p$ each to three volts. On the voltage across the load capacitor $C_l$ and the pump capacitor $C_p$ reaching three volts the charge switches SC1 and SC2 are operated for isolating the pump capacitor $C_p$ from the supply voltage and ground, and for isolating the load capacitor $C_l$ from the supply voltage $V_s$. The first pump switch SP1 is then operated for connecting the second plate of the pump capacitor $C_p$ to the supply voltage $V_s$, thereby raising the voltage of the pump capacitor $C_p$ to six volts, which is then applied through the second pump switch SP2 to

the load capacitor $C_1$, thereby charging and raising the voltage across the load capacitor $C_1$ to six volts. At this stage power up of the charge pump circuit 1 is complete, and the select signal is deactivated on the select pins $P_1$ of the first and second charge switches SC1 and SC2 and the first and second pump switches SP1 and SP2, thereby deselecting the high resistance switches SR1 and selecting the low resistance switches SR2 of the respective switches SC1, SC2, SP1 and SP2. Thereafter, the charge pump circuit operates in a steady state condition, and the voltage across the load capacitor $C_1$ is maintained at six volts by operating the switches SC1, SC2, SP1 and SP2 with their respective low resistance switches SR2 selected and their high resistance switches SR1 deselected. Steady state operation of the charge pump circuit 1 will be well known to those skilled in the art, and is substantially similar to the operation of the circuit 1 during power up just described, with the exception that as the pump capacitor $C_p$ is being charged through the first and second charge switches SC1 and SC2, the second pump switch SP2 is operated for isolating the load capacitor $C_1$ from the supply voltage $V_s$.

In this embodiment of the invention the select signal which is applied to the select pin $P_1$ of each of the switches SC1, SC2, SP1 and SP2 is derived from a

microprocessor in an associated circuit. The select signal, typically a continuous high signal, is applied to the select pins $P_1$ for a predetermined period of time which is of sufficient duration for initially charging the load capacitor $C_1$ to six volts, and typically, is two seconds.

The resistance value of the low resistance switches SR2 is as low as possible, and consistent with integrated circuit technology, in order to provide a substantially resistance free charge and pump paths for facilitating incremental charging of the pump capacitor $C_p$ during steady state operation of the charge pump circuit 1. The resistance of the high resistance switches SR1 is chosen to provide high resistance charge and pump paths, for minimising the current drawn from the supply voltage $V_s$ during initial charging of the load capacitor $C_1$ and the pump capacitor $C_p$. The resistance of the high resistance switches SR1 must also be consistent with initial charging of the load capacitor $C_1$ and pump capacitor $C_p$ within a reasonable time period, typically, up to two seconds. The select signal is arranged in this embodiment of the invention to remain active on the select pins $P_1$ of the switches SC1, SC2, SP1 and SP2 until the load and pump capacitors $C_1$ and $C_p$ are initially charged and the load capacitor $C_1$ is charged to the output voltage. However, it will be appreciated

that instead of applying the select signal for a predetermined period of time, a monitoring circuit may be provided for monitoring the voltage across the load capacitor $C_l$, and on the monitored voltage reaching the desired output voltage $V_h$, the select signal would be deactivated.

It will be appreciated that while the high resistance and low resistance pump path and charge path have been described as being provided by high resistance and low resistance switches, respectively, any other suitable circuitry may be provided for providing a high resistance and a low resistance path in parallel with each other in each of the charge path and the pump path, and any other suitable means for selecting the high resistance and low resistance paths may be provided besides that already described. For example, it is envisaged that a high resistance element such as a resistor may be provided in each high resistance path for forming the high resistance paths, and the desired paths of the high and low resistance paths could be selected by suitable switch means.

It will be appreciated that where the high resistance and low resistance paths are provided by respective high resistance and low resistance switches, the benefits of the invention insofar as reducing the

initial current drawn by the charge pump circuit could be derived by providing only one of the first and second charge switches with respective high and low resistance switches, and the second pump switch SP2 with high and low resistance switches. However, in order to minimise electromagnetic interference and radio frequency interference, it is desirable that both the first and second charge switches and the first and second pump switches should provide high and low resistance paths.

While the initial voltages to which the load capacitor $C_l$ and the pump capacitor $C_p$ are initially charged, have been described as being three volts, it will be appreciated that in practice due to circuit and switch losses, the voltages to which the load and pump capacitors $C_l$ and $C_p$ are charged will be slightly less than the supply voltage, and similarly, the steady state output voltage across the load capacitor $C_l$ will be less than double the supply voltage. Accordingly, in the present case, with a supply voltage $V_s$ of three volts, the pump capacitor $C_p$ and load capacitor $C_l$ will be charged to an initial voltage below three volts, and the normal steady state output voltage across the load capacitor $C_l$ will be slightly below six volts.

Referring now to Fig. 2 there is illustrated a charge

pump circuit which is indicated generally by the reference numeral 10 according to another embodiment of the invention. The charge pump circuit 10 is substantially similar to the charge pump circuit 1, and similar components are identified by the same reference numerals. In this embodiment of the invention the charge pump circuit 10 comprises two pump capacitors, namely, $C_{p1}$ and $C_{p2}$ for providing a voltage across the load capacitor $C_1$ equal to approximately three times the supply voltage, namely, $3V_s$. The pump capacitors $C_{p1}$ and $C_{p2}$ are connected to the supply voltage $V_s$ and ground through respective charge paths, each of which comprises a first charge switch SC1 and second charge switch SC2 in series with the corresponding pump capacitors $C_{p1}$ and $C_{p2}$, for charging the pump capacitors $C_{p1}$ with $C_{p2}$. The pump path in the charge pump circuit 10 comprises two first pump switches SP1 in series with the pump capacitors $C_{p1}$ and $C_{p2}$ as well as the second pump switch SP2 which is also in series with the pump capacitor $C_{p1}$ and $C_{p2}$ and the load capacitor $C_1$.

The first and second charge switches SC1 and SC2 are identical to the first and second charge switches SC1 and SC2 of the charge pump circuit 1 of Fig. 1, and similarly, the first and second pump switches SP1 and SP2 are likewise similar to the first and second pump switches SP1 and SP2 of the circuit 1 of Fig. 1. The

first pump switches SP1 isolate the respective second plates of the pump capacitor $C_{p1}$ and $C_{p2}$ from the supply voltage $V_s$ during charging of the pump capacitors $C_{p1}$ and $C_{p2}$. The second pump switch SP2 isolates the load capacitor $C_1$ from the voltage supply $V_s$ during charging of the pump capacitors $C_{p1}$ and $C_{p2}$. The first and second pump switches SP1 and SP2 connect the pump capacitors $C_{p1}$ and $C_{p2}$ and the load capacitors $C_1$ in series during raising of the voltage on the pump capacitors $C_{p1}$ and $C_{p2}$ and subsequent charging of the load capacitors $C_1$ to the output voltage $V_h$. Additionally, the second pump switch SP2 connects the load capacitor $C_1$ to the supply voltage through the first charge switch SC1 associated with the second pump capacitor $C_{p2}$ during initial charging of the load capacitor $C_1$ to the supply voltage $V_s$.

The operation of the charge pump circuit 10 will be readily apparent to those skilled in the art. Initially, on start-up the high resistance switches SR1 of the switches SC1, SC2, SP1 and SP2 are selected, and initially the pump capacitors $C_{p1}$ and $C_{p2}$ and the load capacitor $C_1$ are charged to the supply voltage $V_s$ by closing the switches SC1, SC2, and SP2, the first pump switches SP1 remaining open. On the pump capacitors $C_{p1}$ and $C_{p2}$ and the load capacitor $C_1$ being charged to the supply voltage $V_s$, the first and second charge switches SC1 and SC2 are opened, and the two first pump switches

SP1 are closed, the second pump switch SP2 remains closed. This, thus raises the voltage on the pump capacitors $C_{p1}$ to twice the supply voltage, namely, $2V_s$, and the voltage on the pump capacitor $C_{p2}$ to three times the supply voltage, namely, $3V_s$. This in turn raises the voltage across the load capacitor $C_l$ to three times the supply voltage, namely, $3V_s$. Steady state operation of the circuit will be well known to those skilled in the art, and will be substantially similar to that described during power up, with the exception that as the pump capacitors $C_{p1}$ and $C_{p2}$ are being simultaneously charged through the first and second charge switches SC1 and SC2, the second pump switch SP2 is open for isolating the load capacitor $C_l$ from the supply voltage $V_s$. Furthermore, during steady operation of the circuit 10 the high resistance switches SR1 are deselected and the low resistance switches SR2 of the switches SC1, SC2, SP1 and SP2 are selected.

The values of the capacitors $C_p$, $C_{p1}$, $C_{p2}$ and $C_l$ are chosen to be consistent with the power requirements from the respective charge pump circuits, and the selection of the capacitor values will be well known to those skilled in the art.

CLAIMS

1. A charge pump circuit comprising at least one pump capacitor, and a load capacitor, a charge path for charging the pump capacitor, and a pump path for charging the load capacitor to an output voltage which is above the supply voltage, wherein each of the charge paths and the pump paths comprises a high resistance path and a low resistance path in parallel with each other, the high resistance and low resistance paths of the respective charge and pump paths being selectively operable so that initial charging of the pump capacitor and initial charging of the load capacitor to the output voltage is through the high resistance paths of the respective pump and charge paths, and charging of the pump capacitor and the load capacitor during steady state operation of the circuit is through the low resistance paths of the respective pump and charge paths.

2. A charge pump circuit as claimed in Claim 1 in which each high resistance path comprises at least one high resistance element.

3. A charge pump circuit as claimed in Claim 1 or 2 in which the charge path comprises a first charge switch means and a second charge switch means in series with the pump capacitor for respectively connecting the

pump capacitor to the supply voltage and to ground for charging the pump capacitor.

4. A charge pump circuit as claimed in Claim 3 in which at least one of the first and second charge switch means comprises a high resistance switch means and a low resistance switch means in parallel with each other for forming the high resistance path and the low resistance path, respectively, of the charge path.

5. A charge pump circuit as claimed in Claim 3 or 4 in which both the first charge switch means and the second charge switch means each comprise a high resistance switch means and a low resistance switch means in parallel with the high resistance switch means for forming the high resistance path and the low resistance path, respectively, of the charge path.

6. A charge pump circuit as claimed in any preceding claim in which the pump path comprises a first pump switch means in series with the pump capacitor and the load capacitor for connecting the pump capacitor to the supply voltage for raising the voltage of the pump capacitor above the supply voltage, for in turn charging the load capacitor to the output voltage.

7. A charge pump circuit as claimed in Claim 6 in

which the first pump switch means comprises a high resistance switch means and a low resistance switch means in parallel with each other for forming the high resistance path and the low resistance path, respectively, of the pump path.

8. A charge pump circuit as claimed in Claim 5 or 6 in which a second pump switch means is provided in series with the pump capacitor and the load capacitor for selectively connecting the respective capacitors together for charging the load capacitor.

9. A charge pump circuit as claimed in Claim 8 in which the second pump switch means comprises a high resistance switch means and a low resistance switch means in parallel with each other for forming the high resistance path and the low resistance path, respectively, of the pump path.

10. A charge pump circuit as claimed in any of Claims 3 to 9 in which each high resistance switch means comprises a high resistance transistor switch, and each low resistance switch means comprises a low resistance transistor switch.

11. A charge pump circuit as claimed in Claim 10 in which the respective high and low resistance transistor

switches are solid state switches.

12. A charge pump circuit as claimed in any of Claims 3 to 11 in which each charge switch means and each pump switch means is responsive to a select signal for simultaneously selecting the high resistance switch means and deselecting the low resistance switch means.

13. A charge pump circuit as claimed in any preceding claim in which a plurality of pump capacitors are connected in series with the load capacitor in the pump path, and each pump capacitor is provided with a charge path having a high resistance path and a parallel low resistance path.

14. A charge pump circuit substantially as described herein with reference to and as illustrated in Fig. 1 of the accompanying drawings.

15. A charge pump circuit substantially as described herein with reference to and as illustrated in Fig. 2 of the accompanying drawings.

16. A circuit comprising the charge pump circuit as claimed in any preceding claim, and a control means for issuing a select signal for selecting one of the high resistance and low resistance paths of the respective

pump and charge paths.

17. A circuit as claimed in Claim 16 in which the control means is implemented in software in a microprocessor, the select signal being provided on an output pin of the microprocessor.

The Patent Office

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**Application No:** GB 9725431.2
**Claims searched:** 1-17

**Examiner:** Brian Ede
**Date of search:** 18 February 1998

## Patents Act 1977
## Search Report under Section 17

**Databases searched:**

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.P): H2F(FCP, FXS, FXT, FXX)

Int Cl (Ed.6): G05F 3/20 G11C 5/14 16/06 H02M 3/07

Other: Online: WPI

**Documents considered to be relevant:**

| Category | Identity of document and relevant passage | | Relevant to claims |
|---|---|---|---|
| A | GB 2244392 A | (MOSAID INC) see Fig 3 | - |
| A P | US 5627739 | (WINBOND ELECTRONICS) see Fig 1 | - |

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|---|---|---|---|
| X | Document indicating lack of novelty or inventive step | A | Document indicating technological background and/or state of the art. |
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